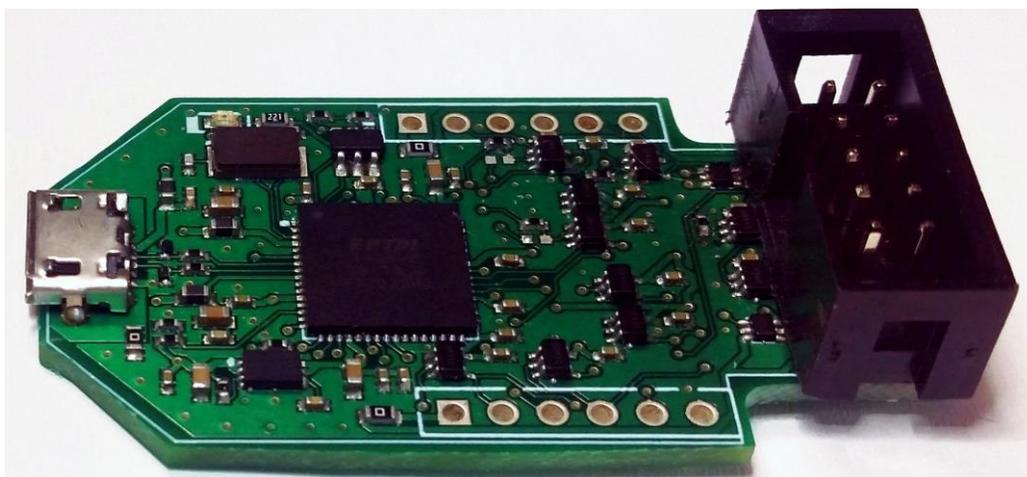


**EPT-2232H-SP-S1****ALTERA JTAG BLASTER****Data Sheet**

The EPT\_2232H\_SP\_S1 is the Altera JTAG Blaster. It is designed to provide JTAG connectivity for Altera devices only. It allows JTAG connectivity of any target voltage from +1.2V to +5V. The target device will provide the voltage and power for the output circuits of the Altera JTAG Blaster. This device connects to an open USB port on a Windows PC and allows the Quartus Programmer application to directly program Altera devices. Installation of the EPT-JTAG-Blaster Driver is required for this device.

**Features:**

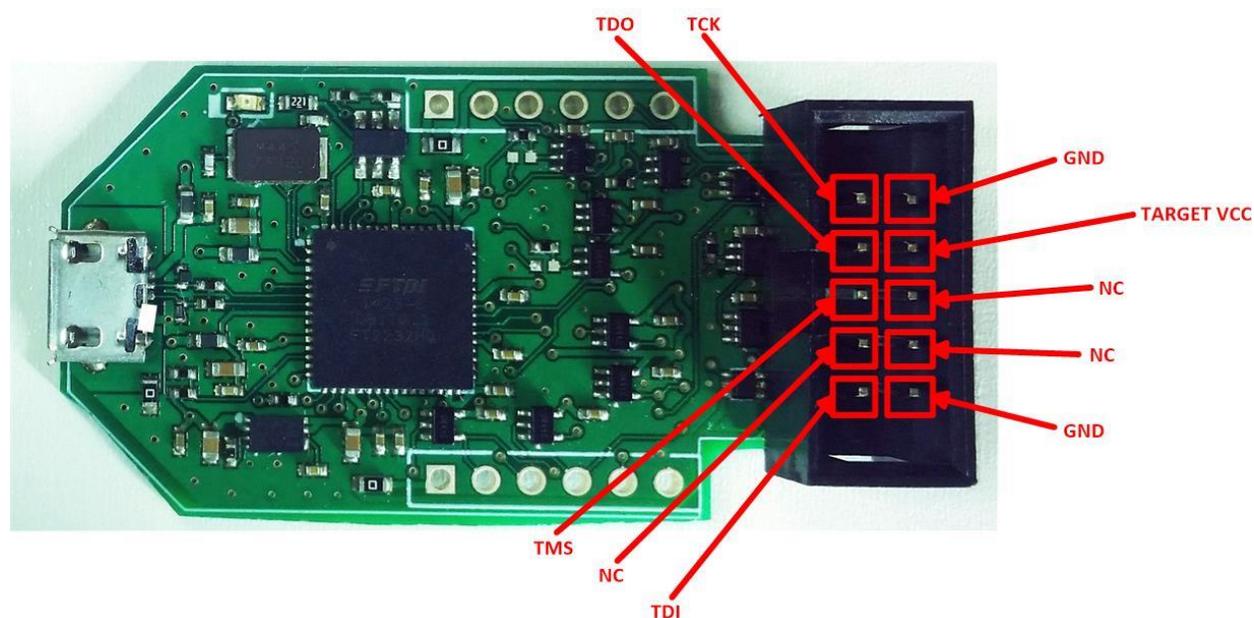
- Programs Altera MAX II, MAX V, MAX10, Cyclone IV, Cyclone V, Stratix IV, Stratix V devices
- Programs JTAG, AS and PS modes
- Works with SignalTap II Logic Analyzer
- Multivolt I/O operation from +1.2V to +5V
- 10 pin header with Altera Standard pinout
- Connect LED indicates USB Enumeration
- Ultra Small footprint
- Micro B USB connector

## 1 Description

Altera JTAG Blaster is powered from the USB cable from a Windows PC. A green LED “Connect” lamp is used to indicate when the board has been enumerated. This means the Windows PC successfully found and installed the USB driver for the board. A separate driver provided by Earth People Technology allows this board to be used by the Quartus Application Programmer. Once this driver has been successfully installed, the device can be found in the Hardware Setup drop down box. Just select the device and the programming mode and the appropriate programming file and the board will program your device.

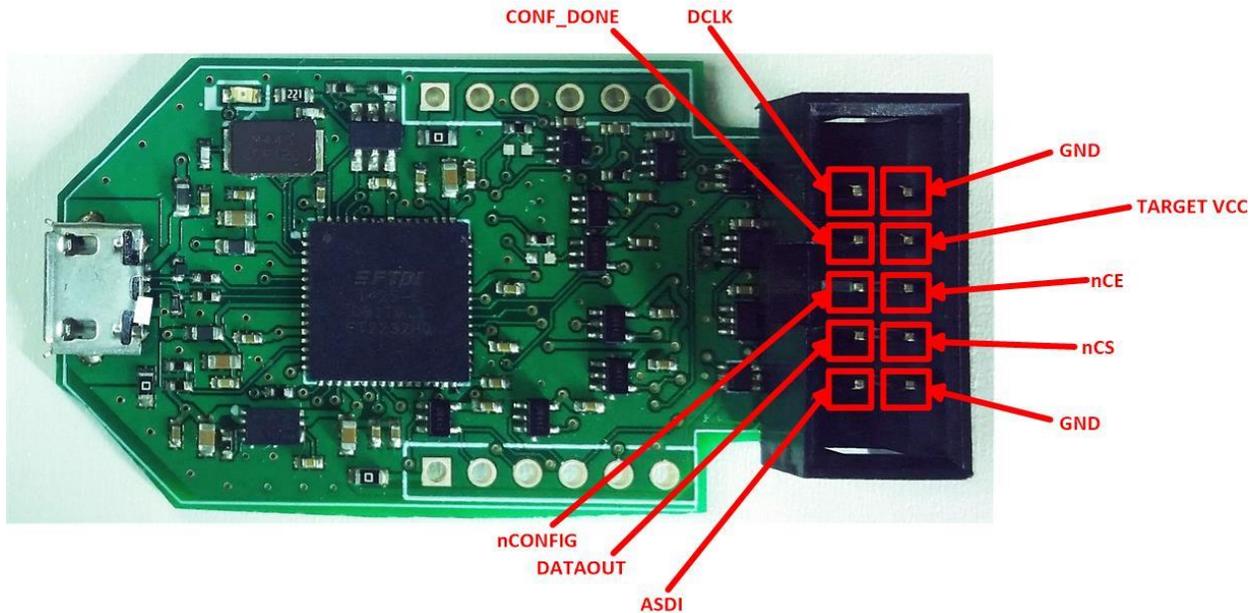
The Altera JTAG Blaster has a 10 pin male header which follows the Altera Standard pinout. It can program Altera devices using the JTAG, AS and PS modes. The JTAG pinout is shown in Figure 1.

Figure 1 EPT-2232H-SP-S1 JTAG Pinout



The pinout for the AS and PS programming modes is shown in Figure 2.

Figure 2 EPT-2232H-SP-S1 AS Pinout



## 2 Mechanical Dimensions

Figure 3 EPT-2232H-SP-S1 Mechanical Dimensions

TBD

## 3 Pin Mapping

Figure 4. Pin Mapping

TBD

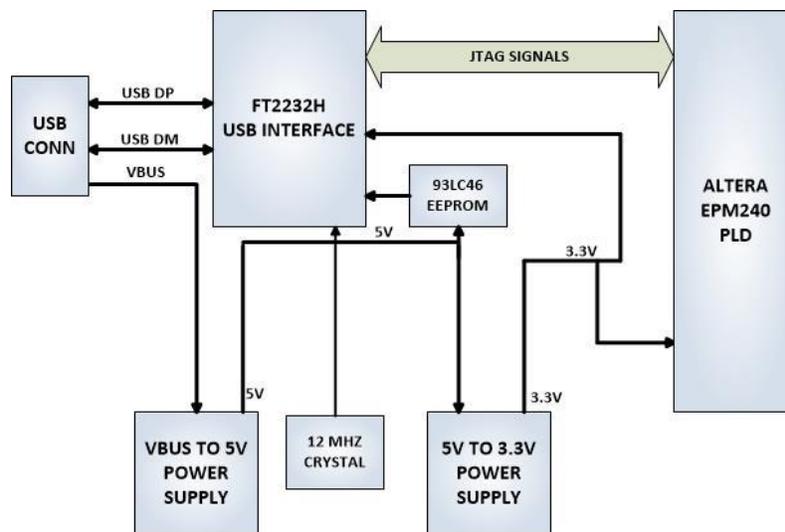
## 4 Inputs/Outputs

. The target device will supply the voltage and power for the output circuits of the Altera JTAG Blaster. The target device must be capable of supplying approximately 12mA (depending of I/O voltage). If the target device does not supply the I/O power or voltage, the Altera JTAG Blaster

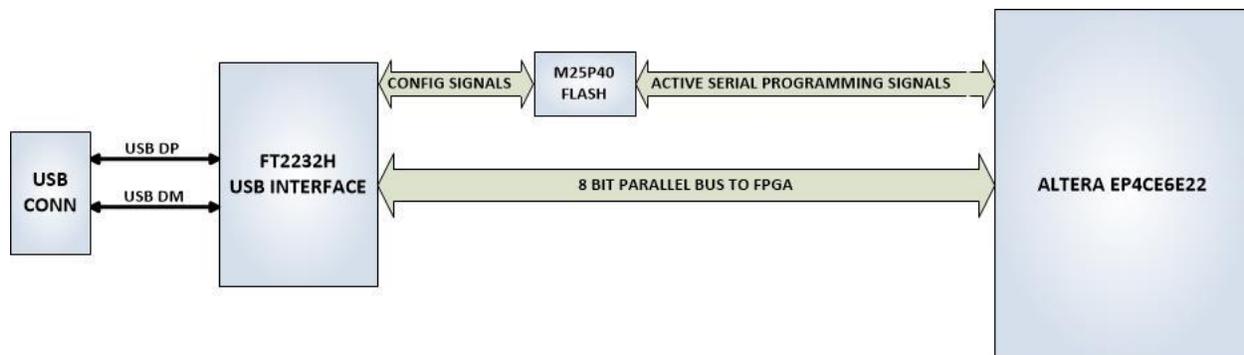
will default to +3.3V output voltage.

## 5 FPGA Configuration

The EPT JTAG Blaster Driver will allow the Quartus II Software to program any Altera Device. This chip is accessed from the FT2232H USB chip. Quartus will store the compiled and synthesized user code.

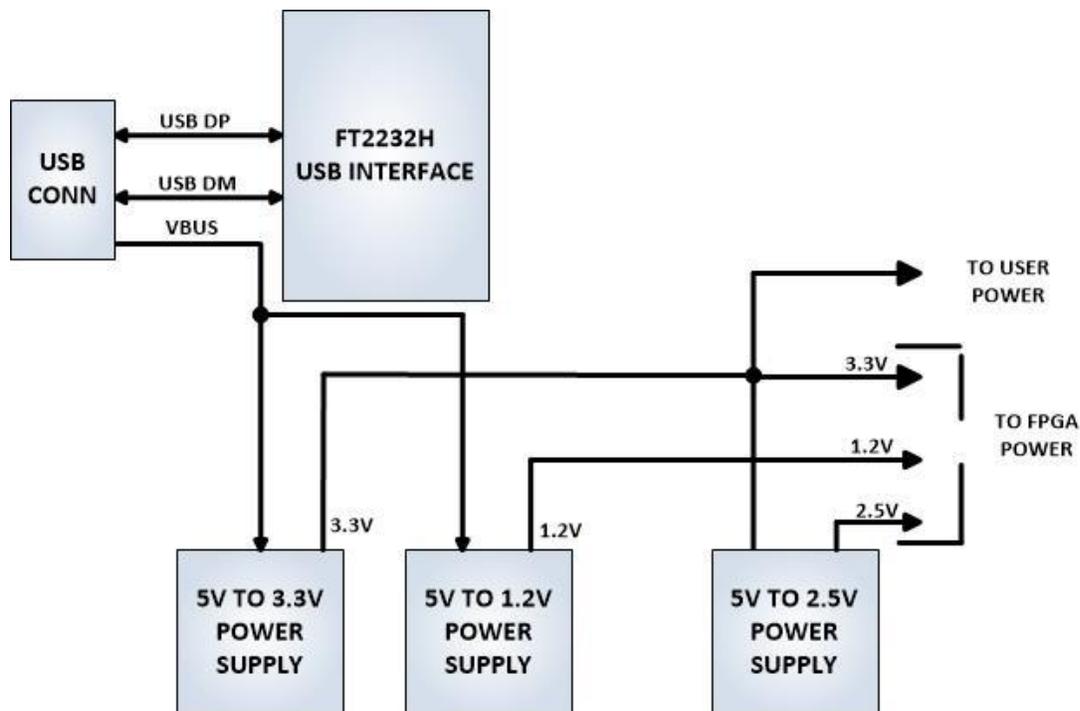


After programming is complete, the FPGA automatically resets and reads the code from the Flash chip and programs itself using the Active Serial method.



## 6 Altera JTAG Blaster Power

The Altera JTAG Blaster is powered from the USB bus of a Host/PC. The USB supplies a maximum of +5V @ 500mA's.



### 1.1.1 Power Budget

Device	Part Number	VUSB		
USB to Serial Chip	FT2232H	70mA		
Voltage Detect Circuit	74LVC1G14SE	1mA		
Power Select Circuit	DMG1023UV	0.1A		

## Data Sheet Altera JTAG Blaster

Voltage Input/Output Drive	74LVC1G17SE	12mA		
<b>Total</b>		<b>82mA</b>		

## 1.1.2 Core Board VUSB Power Budget

Device	Part Number	VUSB		
+3.3V Power Supply	MCP1725-3302	70mA		
<b>Total</b>		<b>70mA</b>		

\* Theoretical Values only. This data needs to be validated