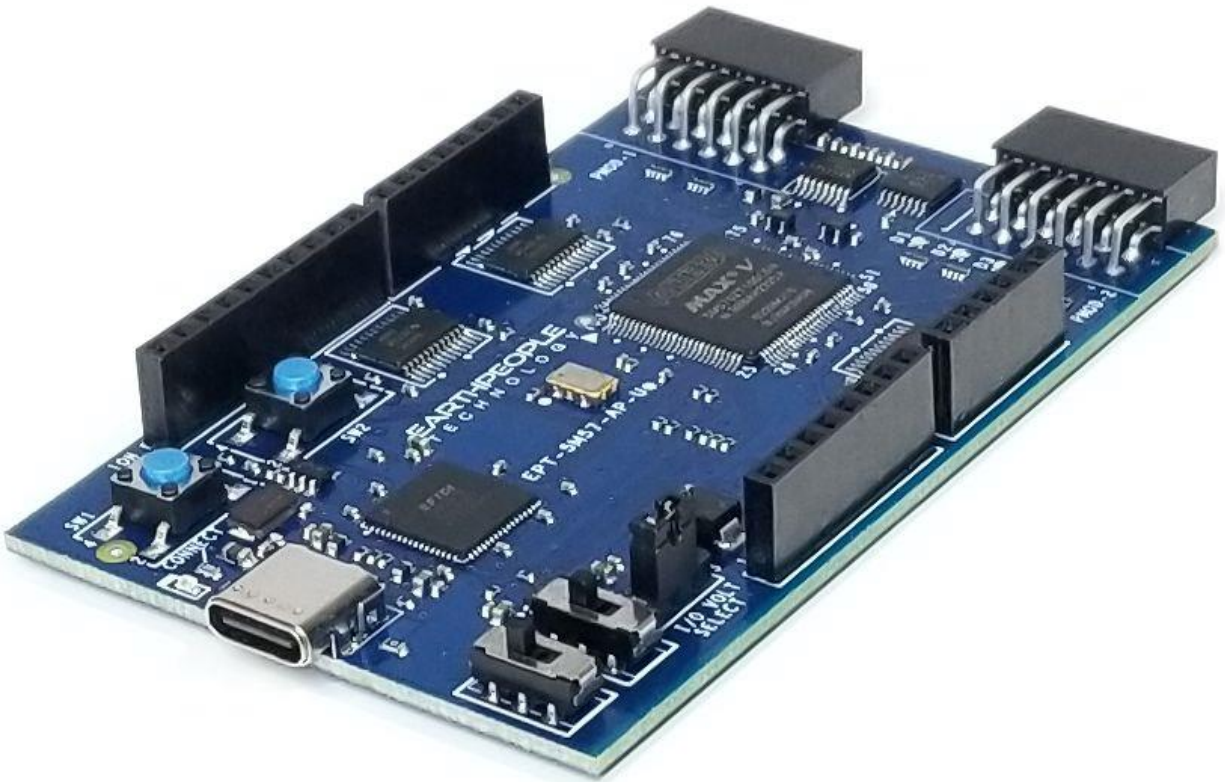UnoMax Development System Data Sheet

UnoMax CPLD Development System

Data Sheet

The UnoMax is a small form factor CPLD Development System. The core functions of the UnoMax are a two channel USB to Serial chip, 570 Logic Cell CPLD and a four channel 300KSample/Sec ADC. The board is powered from a USB port. The Input/Output connectors are designed at the board edge. There are switches to allow the user to experiment with HDL code to read and react to hardware events.

The UnoMax is designed from the ground up as a development board for beginners. All of the

Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin. So, the UnoMax can drive LEDs and sensors directly. The analog inputs have a buffer amp on each input pin. Each Op-Amp on the analog inputs has a 1MHz filter

The board also includes the following parts.

- Intel/Altera 5M570 CPLD with 440 Macrocells
- 4 Channel ADC 300KSamples/Second
- 66 MHz oscillator for driving USB data transfers and users code
- Three bidirectional voltage translator/bus transceivers
- 24 user Input/Outputs available as three 8 bit ports
- Ports have jumper selectable 3.3V/5 Volt Input/Output
- Four RGB LED's accessible by the user
- Two PCB switches accessible by the user
- Two Slide switches accessible by the user
- Two PMOD Connectors

1   Block Diagram

Figure 1-1 UnoMax Component Location

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UnoMax Development System Data Sheet
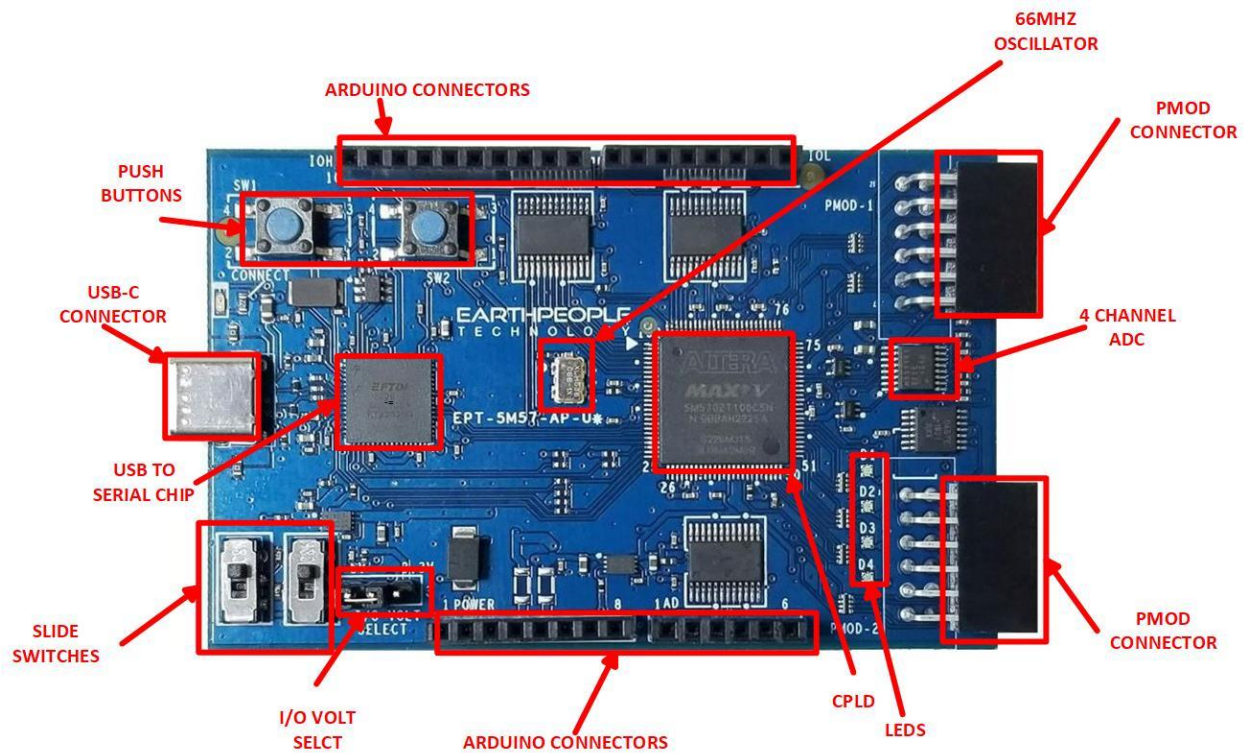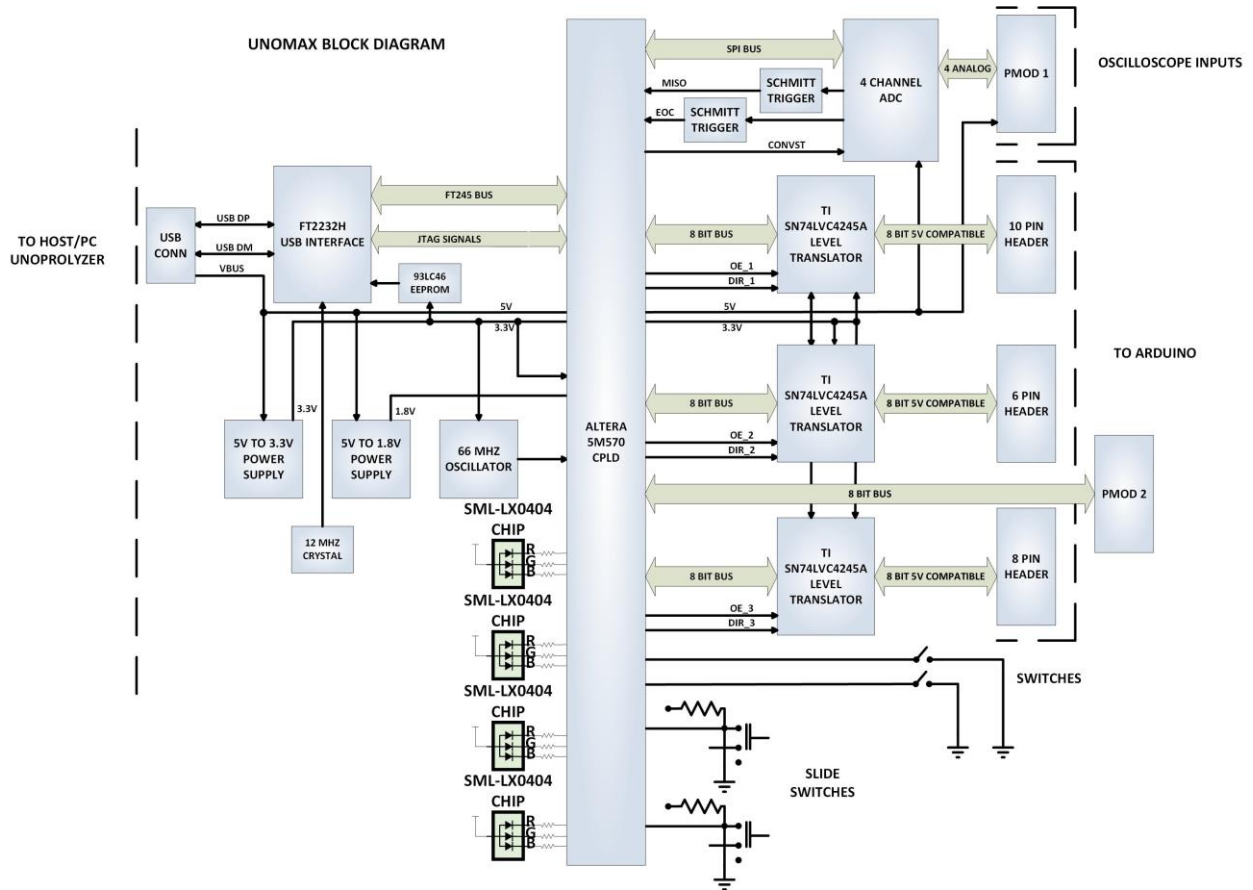

Figure 1-2 UnoMax Block Diagram

EARTHPEOPLE
T e c h n o l o g y

UnoMax Development System Data Sheet

UNOMAX BLOCK DIAGRAM

TO HOST/PC
UNOPROLYZER

USB
CONN

FT2232H
USB INTERFACE

USB DP
USB DM
VBUS

93LC46
EEPROM

FT245 BUS

JTAG SIGNALS

5V
3.3V

SPI BUS

MISO
EOC

SCHMITT
TRIGGER

SCHMITT
TRIGGER

4 CHANNEL
ADC

CONVST

4 ANALOG

PMOD 1

OSCILLOSCOPE INPUTS

8 BIT BUS

TI
SN74LVC4245A
LEVEL
TRANSLATOR

OE_1
DIR_1

5V
3.3V

8 BIT 5V COMPATIBLE

10 PIN
HEADER

5V
3.3V

ALTERA
5M570
CPLD

8 BIT BUS

TI
SN74LVC4245A
LEVEL
TRANSLATOR

OE_2
DIR_2

8 BIT 5V COMPATIBLE

6 PIN
HEADER

TO ARDUINO

3.3V

1.8V

5V TO 3.3V
POWER
SUPPLY

5V TO 1.8V
POWER
SUPPLY

66 MHZ
OSCILLATOR

8 BIT BUS

PMOD 2

12 MHZ
CRYSTAL

SML-LX0404
CHIP

R
G
B

8 BIT BUS

TI
SN74LVC4245A
LEVEL
TRANSLATOR

OE_3
DIR_3

8 BIT 5V COMPATIBLE

8 PIN
HEADER

SML-LX0404
CHIP

R
G
B

SWITCHES

SML-LX0404
CHIP

R
G
B

SLIDE
SWITCHES

SML-LX0404
CHIP

R
G
B

UnoMax Development System Data Sheet

2   Mechanical Dimensions

Figure 2-1 UnoMax Mechanical Dimensions

UNOPROLOGIC PCB DIMENSIONS
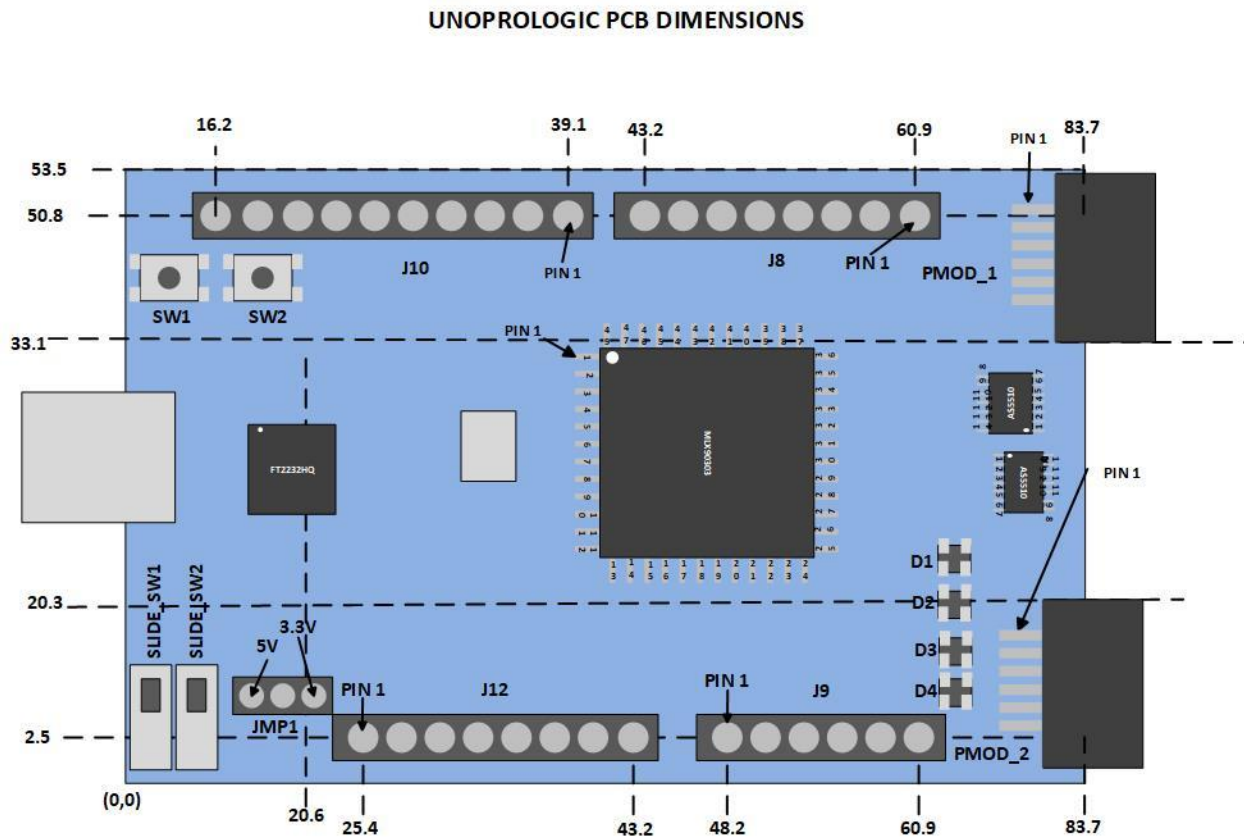
All dimensions in mm

3   Pin Mapping

Component	Pin	Net Name	Pin on CPLD	Signal in EPT Project Pinout

UnoMax Development System Data Sheet

66MHz Oscillator	3	GCLK	12	CLK_66MHZ
Reset	2	NA	44	RST
U12	16	AD0	24	JTAG_TCK (Not In Project)
	17	AD1	23	JTAG_TDI (Not In Project)
	18	AD2	25	JTAG_TDO (Not In Project)
	19	AD3	22	JTAG_TMS (Not In Project)
	38	BD0	19	UART_TX
	39	BD1	18	UART_RX
	NA	NA	17	NA
U7	21	LB7	16	LB_IOH0
	20	LB6	15	LB_IOH1
	19	LB5	7	LB_IOH2
	18	LB4	6	LB_IOH3
	17	LB3	5	LB_IOH4
	16	LB2	4	LB_IOH5
	15	LB1	3	LB_IOH6
	14	LB0	2	LB_IOH7
	NA	NA	1	NA

UnoMax Development System Data Sheet

SW1	1	SW_USER_1	20	SW_USER_1
SW2	1	SW_USER_2	21	SW_USER_23
SW3	1	SLIDE_SWITCH_1	16	SLIDE_SWITCH_1
SW4	1	SLIDE_SWITCH_2	17	SLIDE_SWITCH_2
U7	2	TR_DIR_1	100	TR_DIR_1
U4	2	TR_DIR_2	29	TR_DIR_2
U5	2	TR_DIR_3	85	TR_DIR_3
U7	22	TR_OE_1	86	TR_OE_1
U4	22	TR_OE_2	28	TR_OE_2
U5	22	TR_OE_3	74	TR_OE_3
D1	4	LED_GR_1_N	57	LED_1_GREEN
D1	3	LED_BL_1_N	56	LED_1_BLUE
D1	2	LED_RD_1_N	55	LED_1_RED
D2	4	LED_GR_2_N	54	LED_2_GREEN
D2	3	LED_BL_2_N	53	LED_2_BLUE
D2	2	LED_RD_2_N	52	LED_2_RED
D3	4	LED_GR_3_N	51	LED_3_GREEN
D3	3	LED_BL_3_N	50	LED_3_BLUE
D3	2	LED_RD_3_N	49	LED_3_RED
D4	4	LED_GR_43_N	48	LED_4_GREEN
D4	3	LED_BL_4_N	47	LED_4_BLUE

UnoMax Development System Data Sheet

D4	2	LED_RD_4_N	43	LED_4_RED
U9	16	ADC_EOC	67	ADC_EOC
	12	ADC_CS	68	ADC_CS
	13	ADC_SCLK	69	ADC_CLK
	14	ADC_DIN	70	ADC_MOSI
	15	ADC_DOUT	71	ADC_MISO
	8	ADC_CNVST	72	ADC_CNVST
U5	21	LB16	87	LB_IOL0
	20	LB17	89	LB_IOL1
	19	LB18	91	LB_IOL2
	18	LB19	92	LB_IOL3
	17	LB20	96	LB_IOL4
	16	LB21	97	LB_IOL5
	15	LB22	98	LB_IOL6
	14	LB23	99	LB_IOL7
U4	21	LB8	42	LB_SER0
	20	LB9	41	LB_AD0
	19	LB10	40	LB_AD1
	18	LB11	38	LB_AD2
	17	LB12	36	LB_AD3
	16	LB13	35	LB_AD4

15	LB14	34	LB_AD5
14	LB15	33	LB_SER1
	LB31	58	LB31
	LB32	61	LB32
	LB33	66	LB33
	LB34	62	LB34
	NA	30	NA
	NA	73	NA
	NA	75	NA
	DEV_CLR	44	RESET
	NA	14	NA
	NA	64	NA

4   Pushbutton switches

There are two pushbutton switches on the UnoMax. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.
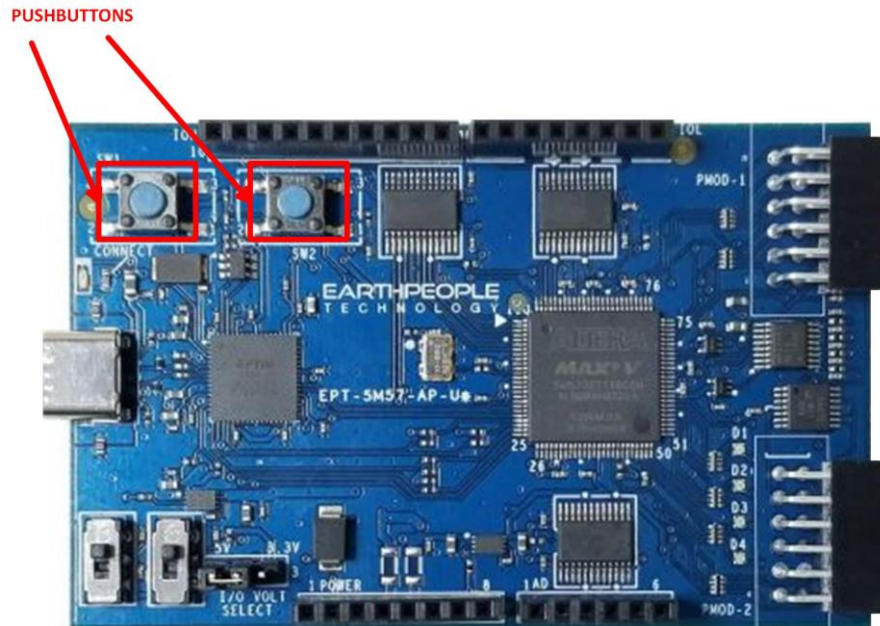
Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
SW1	SW_USER_1	20	SW_USER_1
SW2	SW_USER_2	21	SW_USER_23

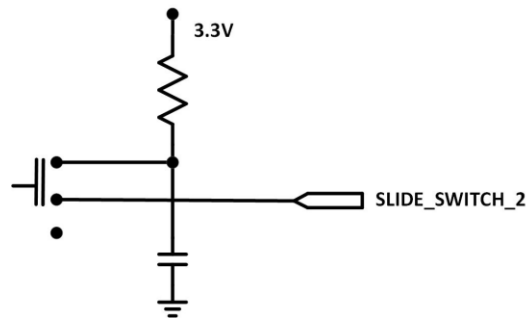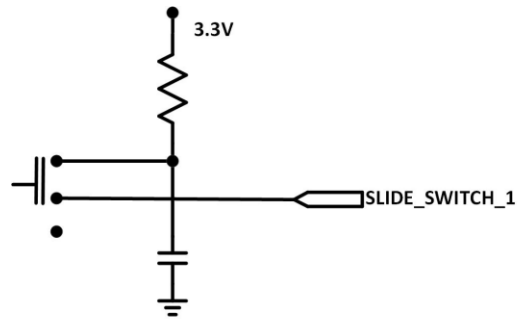UnoMax Development System Data Sheet

PUSHBUTTONS

UnoMax Development System Data Sheet
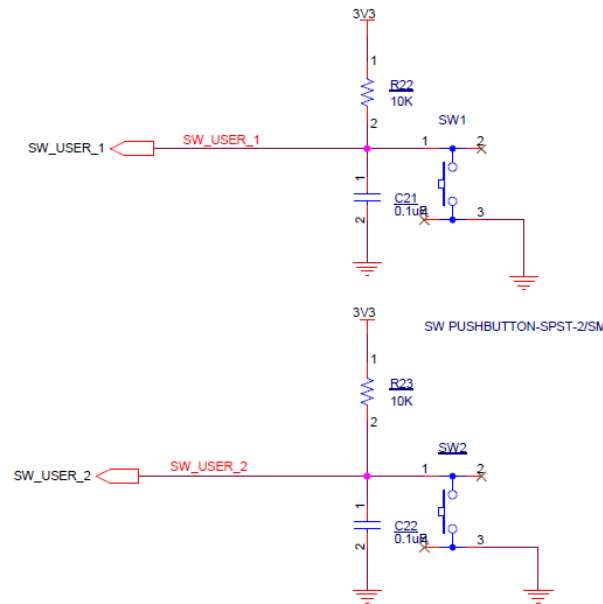
5   Slide Switches

The UnoMax includes two slide switches. Both are full contact switches. They include a 1uF cap to ground to debounce both switches.

EARTHPEOPLE Technology
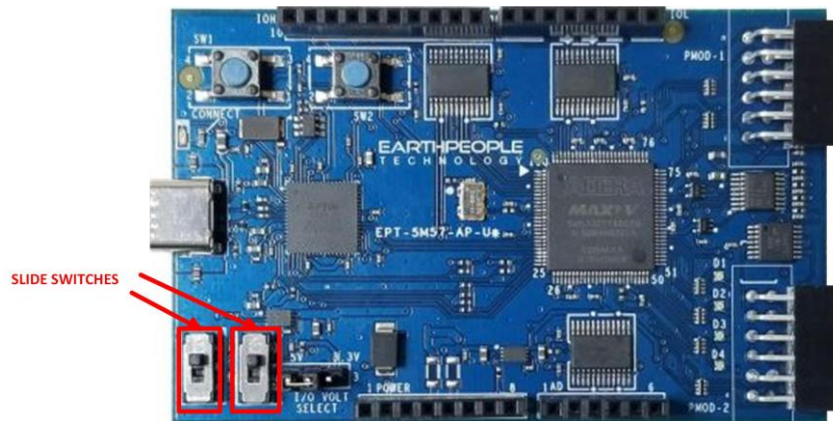
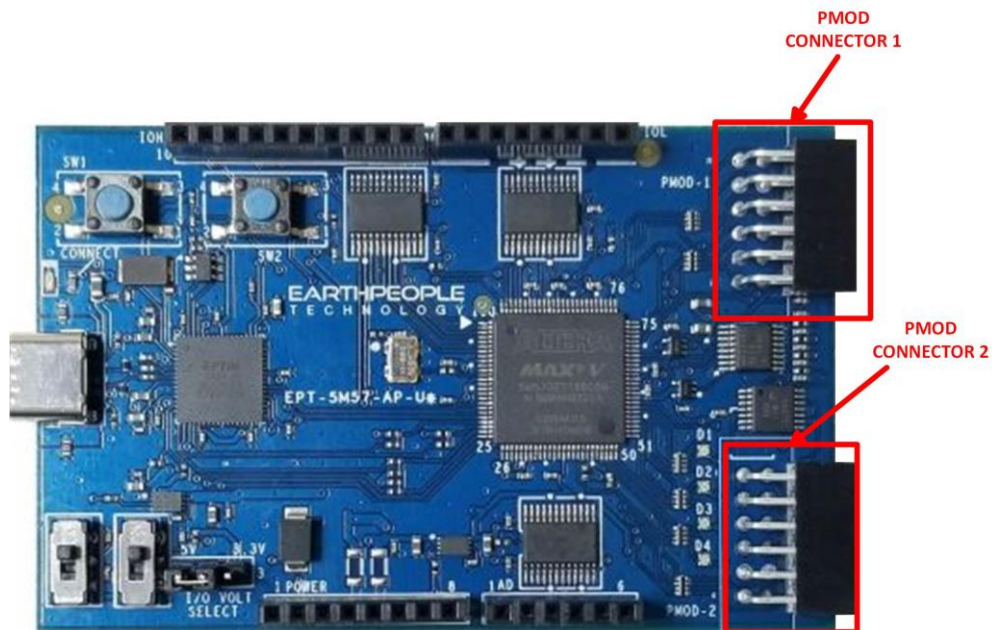UnoMax Development System Data Sheet

| Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
SW3	SLIDE_SWITCH_1	16	SLIDE_SWITCH_1
SW4	SLIDE_SWITCH_2	17	SLIDE_SWITCH_2

6   PMOD Connectors

The UnoMax includes two PMOD Connectors. These two connectors are located towards the rear of the board.

The PMOD pinouts follows the standard pinout. Pin 1 is located in the upper right when facing the connector.

UnoMax Development System Data Sheet
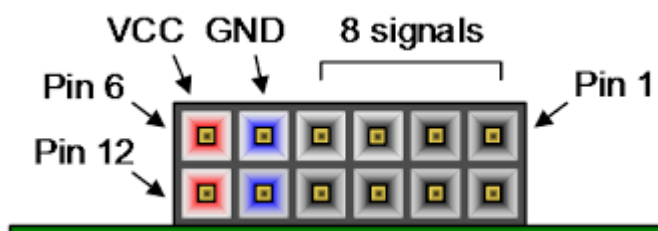
VCC is +3.3V and the Inputs and Outputs of the 8 signals are +3.3V only. The eight I/O's are connected directly to FPGA pins and can be designated as any communications standard.

The PMOD have the following connections to the MAX V chip:

PMOD Pin Number	Signal Name	MAX V Pin Number
1-1	PMOD_1_1	83
1-2	PMOD_1_2	81
1-3	PMOD_1_3	77
1-4	PMOD_1_4	58
1-7	PMOD_1_7	76

| 1-8	PMOD_1_8	78
1-9	PMOD_1_9	82
1-10	PMOD_1_10	84
2-1	ADC_AIN0	NA
2-2	ADC_AIN1	NA
2-3	ADC_AIN2	NA
2-4	ADC_AIN3	NA
2-7	PMOD_2_7	76
2-8	PMOD_2_8	78
2-9	PMOD_2_9	82
2-10	PMOD_2_10	84

7   LEDs

The User LEDs are four RGB LEDs. These LEDs are SML-LX0404 chips and are for use only with +3.3V.

The SML-LX0404 chip is a current sink and are connected to pins on the MAX V CPLD. The anode is connected to +3.3V. The series resistors are calculated for current limiting based on +3.3V.

UnoMax Development System Data Sheet

5M570 CPLD

SML-LX0404 CHIP
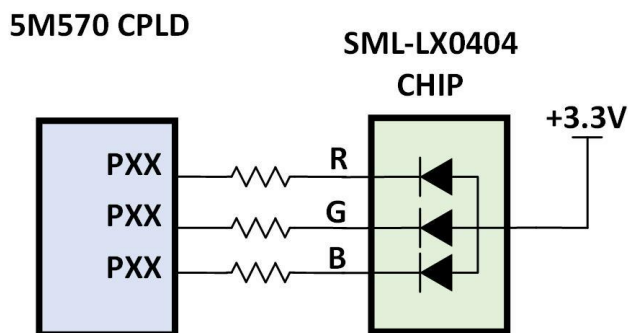
Each series resistor uses a 220 Ohm in a resistor array. In order to light up the each LED, the user code must assert a zero on the associated signal for the LED. To turn off the LED, assert High Z on the signal.

The LED RGB signals are organized on the following pins from the MAX V chip:

LED Number	Signal Name	MAX V Pin Number
D1	LED_GREEN_1_N	57
D1	LED _BLUE_1_N	56
D1	LED_RED_1_N	55
D2	LED_GREEN_2_N	54
D2	LED _BLUE_2_N	53
D2	LED_RED_2_N	52
D3	LED_GREEN_3_N	51
D3	LED _BLUE_3_N	50
D3	LED_RED_3_N	49
D4	LED_GREEN_4_N	48
D4	LED _BLUE_4_N	47
D4	LED_RED_4_N	43

8   Host PC Connection

The UnoMax includes an LED that signifies the connection of the board with the Host PC. The connect LED has the word "CONNECT" in silkscreen next to the LED. This LED will only light up once the Host PC has correctly enumerated the USB device (FT2232HQ chip). When this LED is lit up it can tell the user three things:

- Power has been applied to the UnoMax via USB
- The FT2232HQ chip is working properly
- The Host PC has found the appropriate driver and will communicate with the UnoMax

9   Inputs/Outputs

The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin.

UnoMax Development System Data Sheet

There are 24 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to select which voltage the 24 Inputs/Outputs are set to.

I/O VOLT
SELCT
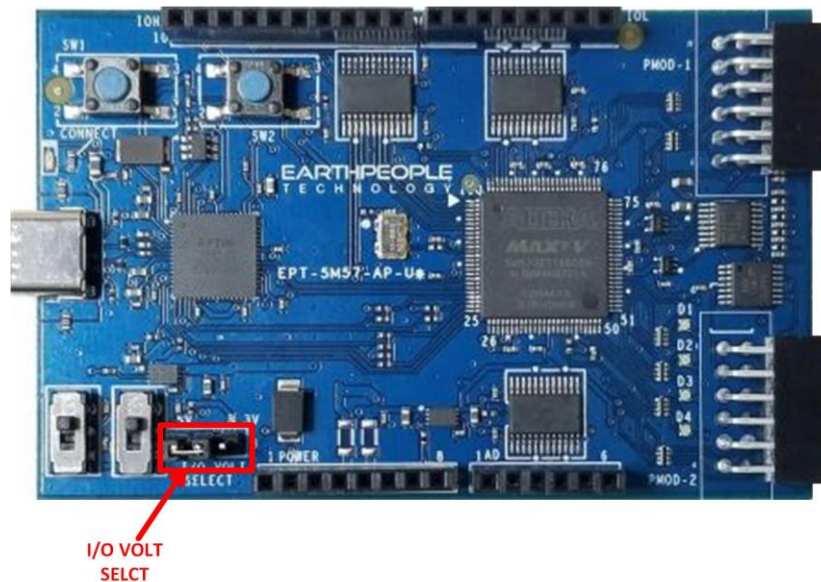
The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will "float".

UnoMax Development System Data Sheet
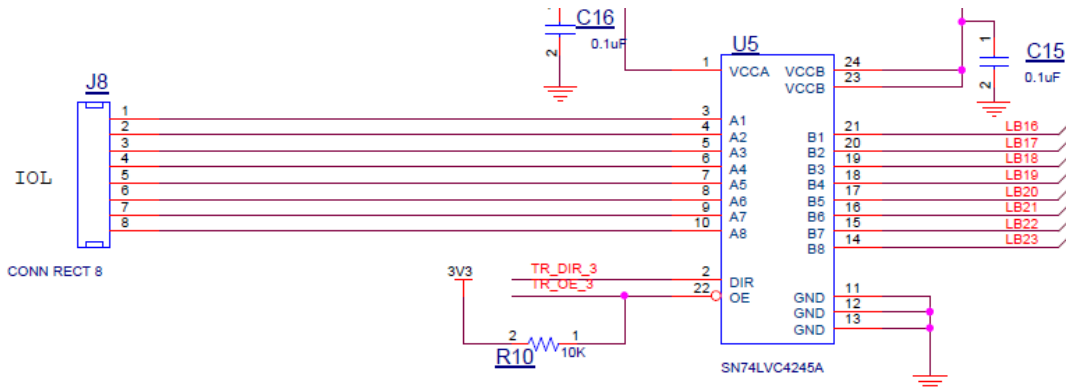
This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has VCCB, which is set at 3.3 V, and A port has VCCA, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, OE) is powered by VCCA.

UnoMax Development System Data Sheet

9.1   Electrical Characteristics

for V_{CCA} = 4.5 V to 5.5 V[1]

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	−40	85	°C

(1)   All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Tim

for V_{CCB} = 2.7 V to 3.6 V[1]

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		−12	mA
		V_{CCB} = 3 V		−24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		−40	85	°C

(1)   All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

9.2   Timing Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

9.3   Description

24 mA drive at 3-V supply
– Good for heavier loads and longer traces
Low VIH
– Allows 3.3-V to 5-V translation

Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

10 Analog connector

The UnoMax includes a six pin analog input connector. This connector provides a path from the pins to the input of the four Op-Amp buffers. Each Op-Amp includes a 1MHz low pass filter.
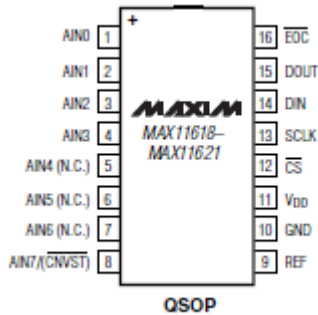
UnoMax Development System Data Sheet

Each Op-Amp provides a buffer for the analog signals to the ADC inputs.
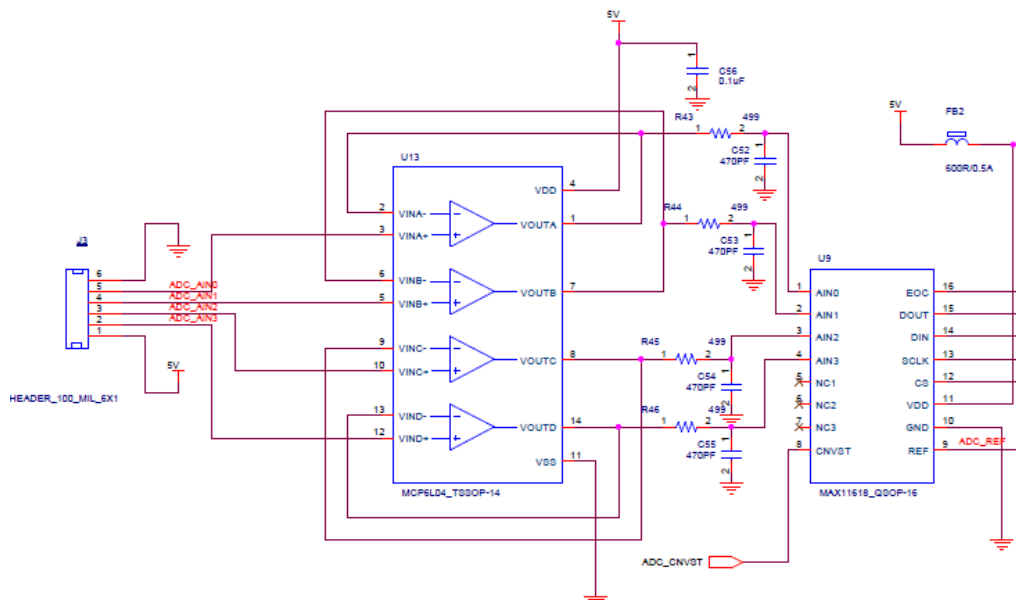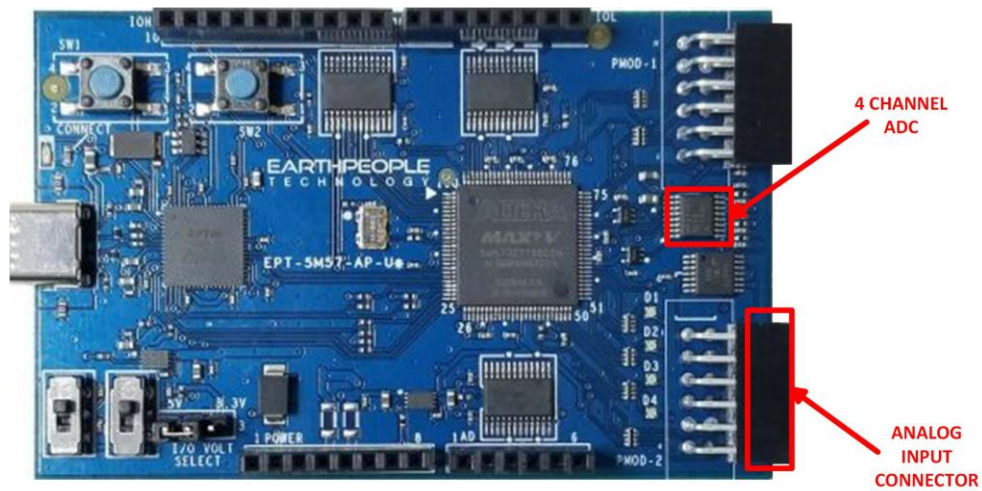
11 Analog to Digital Converter

The EPT 5M57-AP-U2 has an onboard Four Channel, 10 Bit, 300 KSamples/second Analog to Digital Converter. It has a serial SPI communications that allow the host to send setup commands and retrieve the sampled data.

PIN	NAME	FUNCTION
1–4	AIN0–AIN3	Analog Inputs
5, 6, 7	N.C.	No Connection
8	CONVST	Active – low Conversion Start Input
9	REF	Reference Input
10	GND	Ground
11	VDD	Power Input
12	CS	Active Low Chip Select Input. When CS is Low the interface is enabled. When CS is high MOSI is high impedance

13	SCLK	Serial Clock input. Clocks data in and out of the serial interface.
14	MISO	Serial Data input. MISO data is latched into the interface on the rising edge of SCLK
15	MOSI	Serial Data Output. Data is clocked out on the falling edge of SCLK. High impedance when CS is connected to VDD.
16	EOC	End of Conversion Output. Data is valide after EOC pulls low.

11.1 Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference (Note 5)		65		
Acquisition Time	t_{ACQ}		0.6			µs
Conversion Time	t_{CONV}	Internally clocked		3.5		µs
		Externally clocked (Note 6)	2.7			
External Clock Frequency	f_{SCLK}	Externally clocked conversion	0.1		4.8	MHz
		Data I/O			10	
Aperture Delay				30		ns
Aperture Jitter				< 50		ps
ANALOG INPUT						
Input Voltage Range		Unipolar	0		V_{REF}	V
Input Leakage Current		$V_{IN} = V_{DD}$		±0.01	±1	µA
Input Capacitance		During acquisition time (Note 7)		24		pF
INTERNAL REFERENCE						
REF Output Voltage		MAX11618/MAX11620/MAX11624	4.024	4.096	4.168	V
		MAX11619/MAX11621/MAX11625	2.48	2.50	2.52	
REF Temperature Coefficient	TC_{REF}	MAX11618/MAX11620/MAX11624		±20		ppm/°C
		MAX11619/MAX11621/MAX11625		±30		
Output Resistance				6.5		kΩ
REF Output Noise				200		µVRMS
REF Power-Supply Rejection	PSRR			-70		dB
EXTERNAL REFERENCE						
REF Input Voltage Range	V_{REF}		1.0		V_{DD} + 50mV	V
REF Input Current	I_{REF}	V_{REF} = 2.5V (MAX11619/MAX11621/ MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 300ksps		40	100	µA
		V_{REF} = 2.5V (MAX11619/MAX11621/ MAX11625); V_{REF} = 4.096V (MAX11618/MAX11620/MAX11624), f_{SAMPLE} = 0		±0.1	±5	

11.2 3-Wire Serial Interface

The MAX11618–MAX11621/MAX11624/MAX11625 feature a serial interface compatible with SPI/QSPI and MICROWIRE devices. For SPI/QSPI, ensure the CPU serial interface runs in

master mode so it generates the serial clock signal. Select the SCLK frequency of 10MHz or less, and set clock polarity (CPOL) and phase

(CPHA) in the μP control registers to the same value. The MAX11618 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set CS low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. Results are output in binary format.

Serial communication always begins with an 8-bit input data byte (MSB first) loaded from DIN. A high-to-low transition on CS initiates the data input operation. The input data byte and the subsequent data bytes are clocked from DIN into the serial interface on the rising edge of SCLK. Tables 1–5 detail the register descriptions.

Bits 5 and 4, CKSEL1 and CKSEL0, respectively, control the clock modes in the setup register. Choose between four different clock modes for various ways to start a conversion and determine whether the acquisitions are internally or externally timed. Select clock mode 00 to configure CNVST/AIN_ to act as a conversion start and use it to request the programmed, internally timed conversions without tying up the serial bus. In clock mode 01, use CNVST to request conversions one channel at a time, controlling the sampling speed without tying up the serial bus. Request and start internally timed conversions through the serial interface by writing to the conversion register in the default clock mode 10. Use clock mode 11 with SCLK up to 4.8MHz for externally timed acquisitions to achieve sampling rates up to 300ksps. Clock mode 11 disables scanning and averaging.

 The device feature an active-low, end-of-conversion output. EOC goes low when the ADC completes the last requested operation and is waiting for the next input data byte (for clock modes 00 and 10). In clock mode 01, EOC goes low after the ADC completes each requested operation. EOC goes high when CS or CNVST goes low. EOC is always high in clock mode 11.

11.3 Output Data Format
Figures 4–7 illustrate the conversion timing for the MAX11618–MAX11621/MAX11624/MAX11625. The 10-bit conversion result is output in MSB-first format with four leading zeros followed by 10-bit data and two trailing zeros. DIN data is latched into

the serial interface on the rising edge of SCLK. Data on DOUT transitions on the falling edge of SCLK. Conversions in clock modes 00 and 01 are initiated by CNVST. Conversions in clock modes 10 and 11 are initiated by writing an input data byte to the conversion register. Data output is binary.
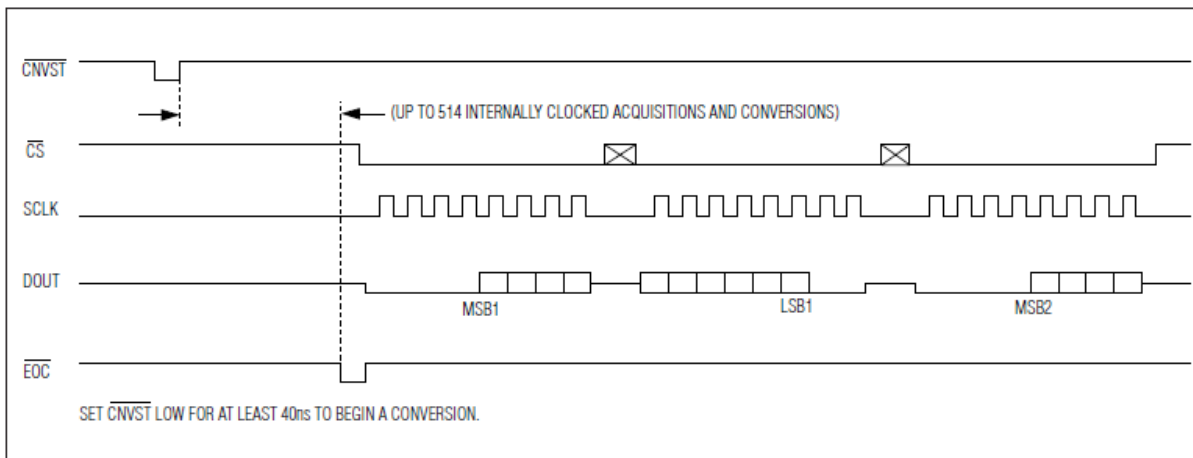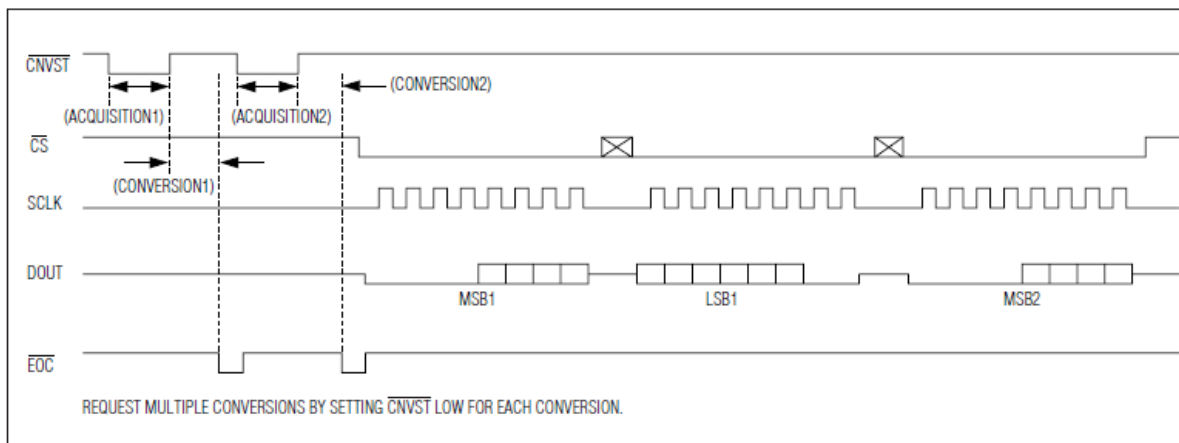

Figure 4. Clock Mode 00

Figure 5. Clock Mode 01
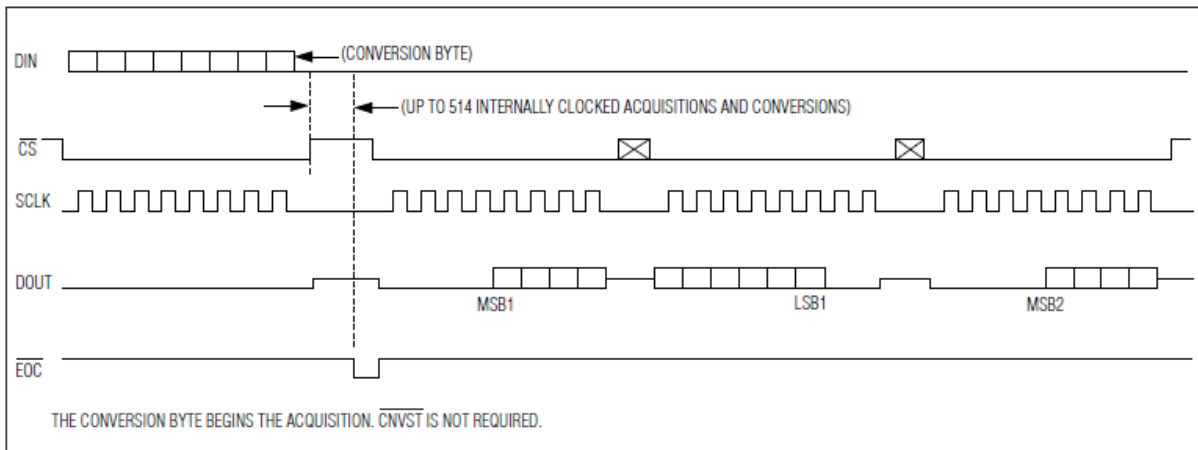
UnoMax Development System Data Sheet
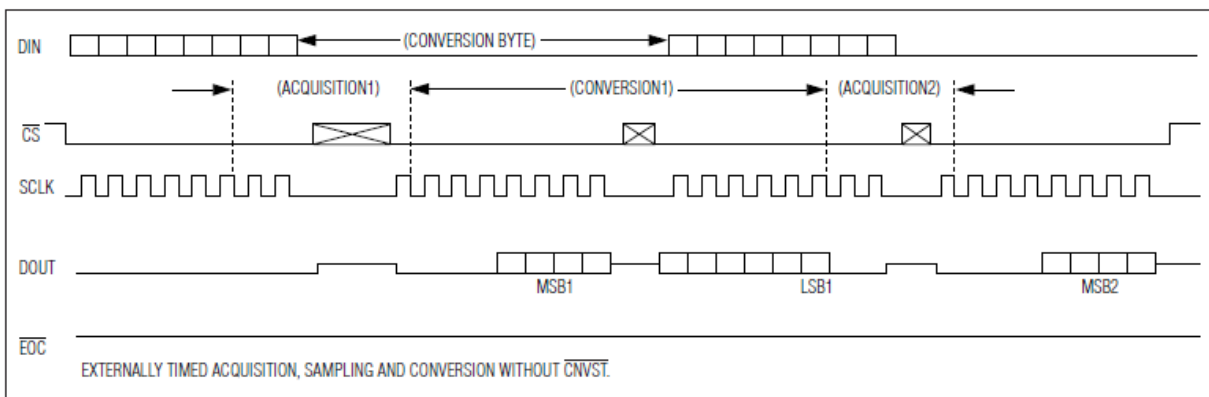

Figure 6. Clock Mode 10

Figure 7. Clock Mode 11

11.4 Register Descriptions

The MAX11618 communicate between the internal registers and the external circuitry through the SPI-/QSPI-compatible serial interface. Table 1 details the registers and the bit names. Tables 2–5 show the various functions within the conversion register, setup register, averaging register, and reset register.

Table 1. Input Data Byte (MSB First)

REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Conversion	1	CHSEL3	CHSEL2	CHSEL1	CHSEL0	SCAN1	SCAN0	X
Setup	0	1	CKSEL1	CKSEL0	REFSEL1	REFSEL0	X	X
Averaging	0	0	1	AVGON	NAVG1	NAVG0	NSCAN1	NSCAN0
Reset	0	0	0	1	$\overline{\text{RESET}}$	X	X	X

X = Don't care.

11.5 Conversion Register

Select active analog input channels per scan and scan modes by writing to the   conversion register. Table 2 details channel selection and the four scan modes.

Request a scan by writing to the conversion register when in clock mode 10 or 11, or by applying a low pulse to the CNVST pin when in clock mode 00 or 01.

A conversion is not performed if it is requested on a channel that has been configured as CNVST. Select scan mode 00 or 01 to return one result per single- ended channel within the requested range. Select scan mode 10 to scan a single input channel numerous times, depending on NSCAN1 and NSCAN0 in the averaging register (Table 4). Select scan mode 11 to return only one result from a single channel.

UnoMax Development System Data Sheet

Table 2. Conversion Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 1 to select conversion register.
CHSEL3	6	Analog input channel select.
CHSEL2	5	Analog input channel select.
CHSEL1	4	Analog input channel select.
CHSEL0	3	Analog input channel select.
SCAN1	2	Scan mode select.
SCAN0	1	Scan mode select.
—	0 (LSB)	Don't care.

CHSEL1	CHSEL0	SELECTED CHANNEL (N)
0	0	AIN0
0	1	AIN1
1	0	AIN2
1	1	AIN3

SCAN1	SCAN0	SCAN MODE (CHANNEL N IS SELECTED BY BITS CHSEL3–CHSEL0)
0	0	Scans channels 0 through N.
0	1	Scans channels N through the highest numbered channel.
1	0	Scans channel N repeatedly. The averaging register sets the number of results.
1	1	No scan. Converts channel N once only.

11.6 Setup Register

Write a byte to the setup register to configure the clock,reference, and power-down modes. Table 3 details the bits in the setup register. Bits 5 and 4 (CKSEL1 and CKSEL0) control the clock mode, acquisition and sampling, and the conversion start. Bits 3 and 2 (REFSEL1 and REFSEL0) control internal or external reference use.

Table 3. Setup Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select setup register.
—	6	Set to 1 to select setup register.
CKSEL1	5	Clock mode and $\overline{\text{CNVST}}$ configuration. Resets to 1 at power-up.
CKSEL0	4	Clock mode and $\overline{\text{CNVST}}$ configuration.
REFSEL1	3	Reference mode configuration.
REFSEL0	2	Reference mode configuration.
—	1	Don't care.
—	0 (LSB)	Don't care.

*See below for bit details.

CKSEL1	CKSEL0	CONVERSION CLOCK	ACQUISITION/SAMPLING	$\overline{\text{CNVST}}$ CONFIGURATION
0	0	Internal	Internally timed	$\overline{\text{CNVST}}$
0	1	Internal	Externally timed through $\overline{\text{CNVST}}$	$\overline{\text{CNVST}}$
1	0	Internal	Internally timed	AIN15/AIN11/AIN7**
1	1	External (4.8MHz max)	Externally timed through SCLK	AIN15/AIN11/AIN7**

**For the MAX11618/MAX11619, $\overline{\text{CNVST}}$ has its own dedicated pin.

REFSEL1	REFSEL0	VOLTAGE REFERENCE	AutoShutdown
0	0	Internal	Reference off after scan; need wake-up delay.
0	1	External single ended	Reference off; no wake-up delay.
1	0	Internal	Reference always on; no wake-up delay.
1	1	Reserved	Reserved. Do not use.

11.7 Averaging Register

Write to the averaging register to configure the ADC to average up to 32 samples for each requested result, and to independently control the number of results requested for single-channel scans. Table 2 details the four scan modes available in the conversion register. All four scan modes allow averaging as long as the AVGON bit, bit 4 in the averaging register, is set to 1. Select scan mode 10 to scan the same channel multiple times. Clock mode 11 disables averaging.

Table 4. Averaging Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 0 to select averaging register.
—	6	Set to 0 to select averaging register.
—	5	Set to 1 to select averaging register.
AVGON	4	Set to 1 to turn averaging on. Set to zero to turn averaging off.
NAVG1	3	Configures the number of conversions for single-channel scans.
NAVG0	2	Configures the number of conversions for single-channel scans.
NSCAN1	1	Single-channel scan count. (Scan mode 10 only.)
NSCAN0	0 (LSB)	Single-channel scan count. (Scan mode 10 only.)

*See below for bit details.

AVGON	NAVG1	NAVG0	FUNCTION
0	X	X	Performs 1 conversion for each requested result.
1	0	0	Performs 4 conversions and returns the average for each requested result.
1	0	1	Performs 8 conversions and returns the average for each requested result.
1	1	0	Performs 16 conversions and returns the average for each requested result.
1	1	1	Performs 32 conversions and returns the average for each requested result.

X = Don't care.

| NSCAN1	NSCAN0	FUNCTION (APPLIES ONLY IF SCAN MODE 10 IS SELECTED)
0	0	Scans channel N and returns 4 results.
0	1	Scans channel N and returns 8 results.
1	0	Scans channel N and returns 12 results.
1	1	Scans channel N and returns 16 results.

11.8 Reset Register

Write to the reset register (as shown in Table 5) to clear the FIFO or to reset all registers to their default states. Set the RESET bit to 1 to reset the FIFO. Set the reset bit to zero to return the MAX11618 to the default power-up state.

Table 5. Reset Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 0 to select reset register.
—	6	Set to 0 to select reset register.
—	5	Set to 0 to select reset register.
—	4	Set to 1 to select reset register.
RESET	3	Set to zero to reset all registers. Set to 1 to clear the FIFO only.
X	2	Don't care.
X	1	Don't care.
X	0 (LSB)	Don't care.

12 MAXV Programming

The UnoMax uses the second channel of the FT2232H chip as a dedicated CPLD programming port. The CPLD must be programmed via JTAG signals and the FT2232H has built in JTAG signals.
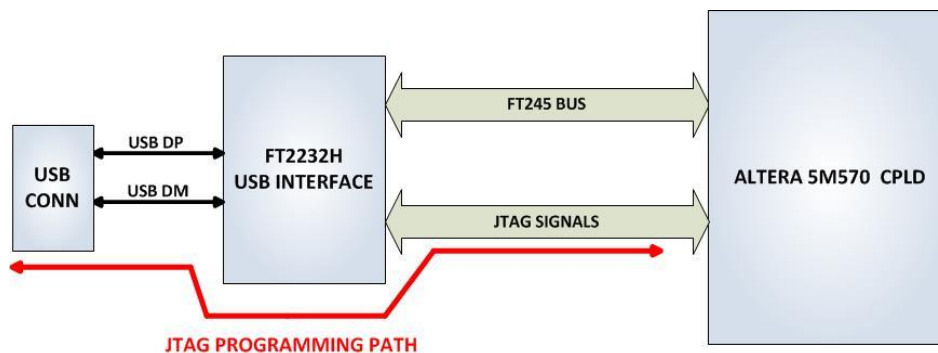
13 Oscillator

There is a 66MHz oscillator on the UnoMax, This oscillator has the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I

This oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling

the net connected to the FPGA pin.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	CLK_66MHZ	

66MHZ OSCILLALTOR
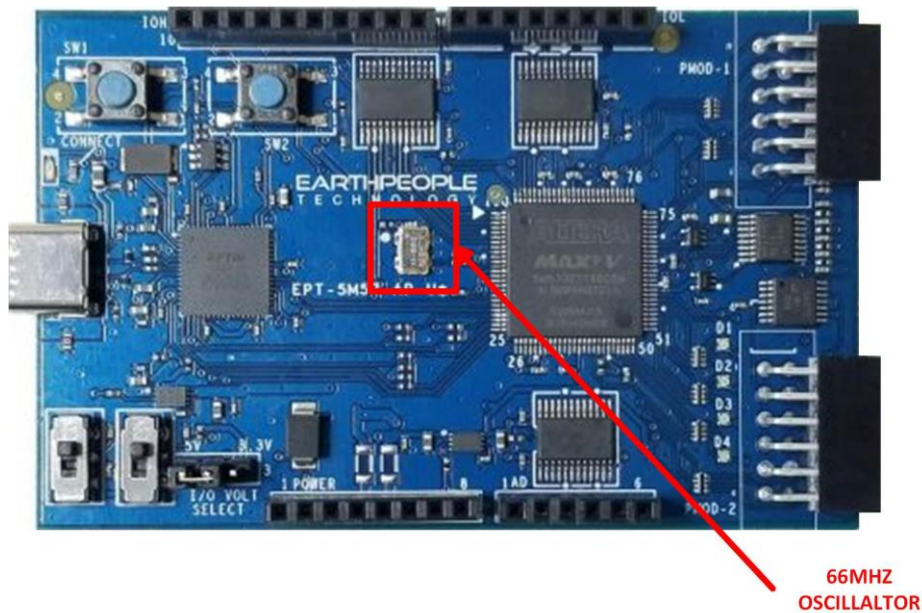
XLH536066.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz

| Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	25 mA
Standby Current	10 µA
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	±25ppm
Operating Temperature	-40°C ~ 85°C

14 USB to Serial

The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is+5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.

15 UnoMax Power

The UnoMax can be powered from the USB bus of a Host/PC or the optional barrel connector. The USB supplies a maximum of +5V @ 500mA's. The components of the UnoMax must share this power with the user code that will run inside the FPGA along with any external power use.
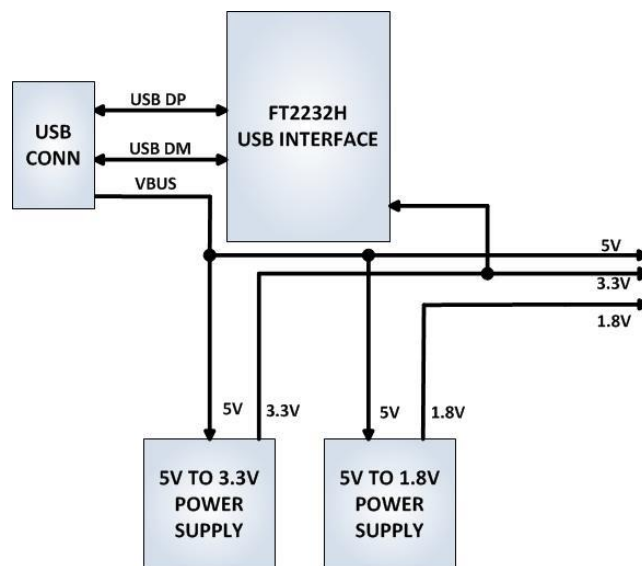
15.1 Core Board Power Budget

Device	Part Number	+1.8V Power	+3.3V Power

CPLD	5M570	??? Defined by user code. EPT-Transfer-Demo code: 50mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Bus Transceivers	74LVC8245		15mA (All eight I/O's active)
USB Chip	FT2232H		60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56		2 mA (write current) 1 mA (read current)
66MHz Oscillator	CB3LV-3I-66M0		10 mA
ADC Four Channel	MAX11618EEE+		17 mA
Op-Amp driver	MCP6L04		0.5 mA (all four amps active)
Schmitt Buffer	74LVC1G17SE		1mA
User LEDs			20 mA

Total		50mA	175.5mA

*Theoritical Values only. This data needs to be validated

15.2 Core Board VUSB Power Budget

Device	Part Number	VUSB		
+1.8V Power Supply	MCP1725-1802E	70mA		
+3.3V Power Supply	MCP1725-3302E	215mA		
Total		**285mA**		

* Theoritical Values only. This data needs to be validated